Remarks

Rejections Under 35 U.S.C. § 102(b)

The Examiner has rejected claims 1-6 and 10-11 under 35 U.S.C. § 102(b) as anticipated by United States Patent number 5,812,803 issued to Pawlowski et al (hereinafter referred to as Pawlowski). The Applicants respectfully request careful consideration of the following arguments in support of the traversal of the Examiner's rejections under 35 U.S.C. § 102(b).

Column 15, line 64 to column 16, line 1 of Pawlowski teaches the following: **line 64-line 1**–"The first value is provided in T1 through T6, which identifies the read buffer used for the first read request." The Examiner asserts that the limitations recited in claim 1 of "generating ***a first value*** using the signal" (emphasis added) read upon the subject matter disclosed in column 15, line 64 through column 16, line 1. Additionally, the Examiner appears to assert that the limitations recited in claim 10 of "**the second value**" (emphasis added) read upon the subject matter disclosed in column 15, line 64 through column 16, line 1.

However, as can be seen from claim 1, claim 1 includes the limitations of "storing the first value in a storage device, with ***the first value including a plurality of bits indicating a beginning of usage of the bus and an ending of the usage of the bus for the transaction in terms of clock cycles***". (emphasis added) And, as can be seen from claim 10, claim 10 includes the limitations of "a storage device to store ***a second value including a first plurality of bits for indicating a beginning of the first data on the bus and an ending of the first data on the bus in terms of the clock cycles***". (emphasis added)

The Applicants respectfully contend that the term "first value" found and described in column 15, line 64 through column 16, line 1 has no relationship to the limitations of claim 1 and claim 10 previously mentioned in this paragraph. "***First value***" in column 15, line 64 "***identifies the read buffer used***". (emphasis added) There is no teaching or suggestion that the first value of column 15, line 64 is used for "indicating a beginning of usage of the bus and an ending of the usage of the bus for the transaction in terms of clock cycles" or "indicating a beginning of the first data on the bus and an ending of the first data on the bus in terms of the clock cycles." Identifying the read buffer to be used

does not teach or suggest "a first value including a plurality of bits indicating a beginning of usage of the bus and an ending of the usage of the bus".

The Examiner asserts that the limitations recited in claim 1 of "storing the first value in a storage device, with ***the first value including a plurality of bits indicating a beginning of usage of the bus and an ending of the usage of the bus for the transaction in terms of clock cycles***" (emphasis added) read upon the subject matter disclosed in column 14, lines 44-64 of Pawlowski. In addition, the Examiner appears to assert that limitations recited in claim 10 of "a bus management device arranged to receive a first value from the memory controller indicating a number of clock cycles with the first data on the bus and including a storage device to store ***a second value including a first plurality of bits for indicating a beginning of the first data on the bus and an ending of the first data on the bus in terms of the clock cycles***" (emphasis added) read upon the subject matter disclosed in column 14, lines 44-64 of Pawlowski. The Applicants respectfully contend that the cited section from Pawlowski does not teach or suggest these limitations of claim 1 and claim 10. The Examiner does not explicitly state what correspondence is asserted between the limitations of claim 1 and claim 10 recited in the paragraph before last and the disclosure of column 14, lines 44-64 in Pawlowski. So, in these remarks, the Applicants are left to make inferences about what the asserted correspondence intended by the Examiner might be.

Column 14, lines 44-64 of Pawlowski teach, among other things, the following:
lines 44-46–"FIG. 5 is a timing diagram showing the timing of the interchip signals for a memory read transaction according to one embodiment of the present invention."
lines 51-54–"The memory read request is placed on the bus by an agent in T1, and is clocked in DC 127 in T2. DC 127 decodes the request and transfers the request into its request queue."
lines 56-58–"the request is immediately transferred to the memory controller of DC 127 which asserts the column memory address on MA[11:0] for the read request in T3."
lines 58-60–"DC 127 then asserts the CAS# signal in T4, indicating that the address on MA[11:0] is the column address.

Because claim 1 recites the act of "storing" and claim 10 recites the element of a "storage device to store", it appears that the Examiner might be asserting a correspondence between these limitations of claim 1 and claim 10 and column 14, lines

51-54, "The memory read request is placed on the bus by an agent in T1, and is clocked in DC 127 in T2. DC 127 decodes the request and transfers the request into its request queue." If that is the case, ***the Examiner would appear to be asserting that "DC 127" corresponds to the "storage device" and the "memory read request" would therefore, it seems, be asserted to correspond to "the first value" of claim 1 and the "second value" of claim 10*** (even though this appears to contradict the correspondence asserted by the Examiner in the previous lines of this same paragraph of the office action). But, in lines 56-58, Pawlowski teaches that this "request is immediately transferred to the memory controller of DC 127 which asserts the column memory address on MA[11:0] for the read request in T3."

The Applicants respectfully contend that this does not teach or suggest the limitations of claim 1 of "***the first value including a plurality of bits indicating a beginning of usage of the bus and an ending of the usage of the bus for the transaction in terms of clock cycles***" or the limitations of claim 10 of "***a second value including a first plurality of bits for indicating a beginning of the first data on the bus and an ending of the first data on the bus in terms of the clock cycles.***" This "request" is used by the "memory controller of DC 127" to assert "the column memory address on MA[11:0]", not to indicate "a ***beginning*** of the usage of the bus and the ***ending*** of the usage of the bus" and not to indicate "a ***beginning*** of the first data on the bus and an ***ending*** of the first data on the bus."

According to MPEP section 2131, "A claim is anticipated only if ***each and every element*** as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." (emphasis added) Because the sections of Pawlowski cited by the Examiner do not teach or suggest "each and every element" as set forth in claim 1 and claim 10, claim 1 and claim 10 are not anticipated under 35 U.S.C. § 102(b). Therefore, the Applicants respectfully request withdrawal of the rejections of claim 1 and claim 10 under 35 U.S.C. § 102(b) based upon Pawlowski.

Claims 2-6 are dependent upon claim 1, either directly or indirectly, and therefore incorporate by reference all the limitations of claim 1. Therefore, the Applicants respectfully request withdrawal of the rejections of claims 2-6 under 35 U.S.C. § 102(b) based upon Pawlowski. As a separate grounds of non-anticipation by Pawlowski, the Applicants respectfully contend that each of claims 2-6 include limitations not taught or

suggested by Pawlowski. Claim 11 is dependent upon claim 10 and therefore incorporates by reference all the limitations of claim 10. Therefore, the Applicants respectfully request withdrawal of the rejection of claim 11 under 35 U.S.C. § 102(b) based upon Pawlowski. As a separate grounds of non-anticipation by Pawlowski, the Applicants respectfully contend that claim 11 includes limitations not taught or suggested by Pawlowski.

Rejections Under 35 U.S.C. § 103(a)

The Examiner has rejected claims 7-9 and 12 under 35 U.S.C. § 103(a) as obvious in view of Pawlowski over United States Patent number 5,581,782, issued to Sarangdhar et al (hereinafter referred to as Sarangdhar). According to MPEP 2143, one element that must be met to make a valid prima facie obviousness rejection is that "the prior art reference (or references when combined) must teach or suggest ***all the claim limitations.***" Claims 7-9 depend indirectly upon claim 1 and therefore incorporate all the limitations of claim 1. Because Pawlowski does not teach or suggest all the limitations of claim 1, a valid prima facie obviousness rejection of claims 7-9 has not been established. Accordingly, the Applicants respectfully request withdrawal of the rejections of claims 7-9 under 35 U.S.C. § 103(a). As a separate grounds of non-obviousness over the cited references, the Applicants respectfully contend that because Pawlowski and Sarangdhar do not, in combination, teach or suggest all the limitations of each of claims 7-9, a valid prima facie obviousness rejection of claims 7-9 has not been established.

Claim 12 depends indirectly upon claim 10 and therefore incorporates all of the limitations of claim 10. Because Pawlowski does not teach or suggest all the limitations of claim 10, a valid prima facie obviousness rejection of claim 12 has not been established. Accordingly, the Applicants respectfully request withdrawal of the rejection of claim 12 under 35 U.S.C. § 103(a). As a separate grounds of non-obviousness over the cited references, the Applicants respectfully contend that because Pawlowski and Sarangdhar do not, in combination, teach or suggest all the limitations of claim 12, a valid prima facie obviousness rejection of claims 12 has not been established.

Objections to the Claims

The Examiner has objected to claims 13-15 as containing allowable subject matter but dependent upon a rejected base claims. The Applicants respectfully request that the objections to claims 13-15 be held in abeyance until a decision is made on the allowability of the rejected base claims.

Allowable Subject Matter

The Examiner has indicated that claims 16-21 are allowed.

Objections to the Abstract

The Applicants have amended the abstract to overcome the Examiner's objections to the length of the abstract. Therefore, the Applicants respectfully request withdrawal of the objection to the abstract.

Conclusion

The Applicants respectfully contend that the subject application is in a condition for allowance. Allowance is respectfully requested.

Respectfully submitted,
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